Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A memory system, comprising:

a control circuit having a data register for storing write data, said control circuit controlling write operation of the memory system; and

memory means having a plurality of memory cells, for latching a data group composed of data of predetermined bits transferred from the data register, for writing the latched data group in the memory cells, and for outputting a collective verify signal when all the data of the data group have been written;

wherein whenever the collective verify signal is outputted by said memory means, said control circuit transfers a new data group to said memory means to allow said memory means to latch and write the transferred new data group therein and transfers the collective verify signal to said control circuit whenever the new latched data group has been written, the write operation being repeated in sequence.

Claims 2-27 (Canceled)